



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,168	04/13/2004	Nhon Toai Quach	42P5725C	3735

8791 7590 08/24/2007
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER

LAMARRE, GUY J

ART UNIT	PAPER NUMBER
----------	--------------

2112

MAIL DATE	DELIVERY MODE
-----------	---------------

08/24/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/823,168

Applicant(s)

QUACH ET AL

Examiner

Guy J. Lamarre

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/19/2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

* The non-statutory double patenting rejection of record is withdrawn in response to the timely filed terminal disclaimer.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1.1 **Claims 1-6, 22-24** are rejected under 35 U.S.C. 101 as claiming non-statutory subject matter: a data signal; such data signal further being devoid of a useful result.

Claim Rejections - 35 USC ' 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) The invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.1. **Claims 1-24** are rejected under 35 U.S.C. 102 (b or a) as being unpatentable over **Liu et al.** "Adaptive source rate control for real-time wireless video transmission; Mobile Networks and Applications, pp 49-60, 1998 (before or after Mar. 27, 1998)," IDS of 6/01/04.

As per **Claim 1**, **Liu et al.** discloses the procedure for the claimed computer or network or communication data signal embedded in one of a machine readable or network or communication device and a machine readable or network or communication medium comprising: a first code group having a first symbol and an error detection code for the first symbol; and a second code group having a second symbol different from the first symbol and an error correction code for a third symbol that includes the first symbol and the second symbol. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig.

Art Unit: 2112

1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 2, Liu et al. discloses the procedure for the claimed computer data signal of claim 1 wherein the third symbol further includes the error detection code. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects

an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 3, Liu et al. discloses the procedure for the claimed computer data signal of claim 1 wherein the computer data signal further comprises a plurality of second code groups, each of said plurality of second code groups containing one of a plurality of second number of bits and one of a plurality of sets of error correction bits for the first number of bits and the one of the plurality of second number of bits. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction

Art Unit: 2112

such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 4, Liu et al. discloses the procedure for the claimed computer data signal of claim 1 wherein the error correction code provides error correction information for the first symbol if the error detection code indicates an error, and error correction information for the second symbol otherwise. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of

said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 5, Liu et al. discloses the procedure for the claimed computer data signal of claim 1 wherein the error detection code is a parity bit. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but

is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 6, Liu et al. discloses the procedure for the claimed computer data signal of claim 1 wherein the error detection code is a plurality of parity bits, where each of said plurality of parity bits can detect an error in a predetermined portion of the first symbol. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 7, Liu et al. discloses the procedure for the claimed method for transmitting correctable data comprising: receiving information data having a first symbol and a

Art Unit: 2112

second symbol different from the first symbol; generating error detection data for the first symbol; transmitting the first symbol and the error detection data; generating error correction data for the first symbol and the second symbol; and transmitting the second symbol and the error correction data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 8, **Liu et al.** discloses the procedure for the claimed method of claim 7 wherein generating error correction data further comprises generating error correction data for the error detection data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a

second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 9, Liu et al. discloses the procedure for the claimed method of claim 7 wherein the information data is further comprised of a plurality of second symbols, and the method further comprises generating error correction data for the first symbol and one of the plurality of second symbols, and transmitting said one of the plurality of second symbols and said error correction data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 10, Liu et al. discloses the procedure for the claimed method of claim 7 wherein the error correction data includes the error detection data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 11, Liu et al. discloses the procedure for the claimed method for receiving correctable data comprising: receiving a first transmitted code group having a first information symbol and error detection data for the first transmitted code group; detecting an error in the first transmitted code group; if the error is not detected providing the first information symbol as a first valid information symbol; otherwise receiving a second transmitted code group having a second information symbol different from the first information symbol and error correction data for the first information symbol and the second transmitted code group, performing error correction on the first and second information symbols, and providing the first information symbol as the first valid information symbol after performing error correction. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction

Art Unit: 2112

such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 12, Liu et al. discloses the procedure for the claimed method of claim 11 wherein performing error correction includes performing error correction on the error detection data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of

Art Unit: 2112.

said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 13, Liu et al. discloses the procedure for the claimed method of claim 11 wherein receiving the second transmitted code group further comprises receiving one of a plurality of second transmitted code groups, each of said plurality of second transmitted code groups comprised of one of a plurality of second information symbols and one of a plurality of error correction data for said first information symbol and said one of a plurality of second transmitted code groups. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 14, Liu et al. discloses the procedure for the claimed of claim 11 wherein the error correction data includes the error detection data. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 15, Liu et al. discloses the procedure for the claimed data transmission device comprising: a first register that receives a first number of bits; a second register that receives a second number of bits different from the first number of bits; an error detection generator coupled to the first register that generates an error detection bit for the first number of bits; an error correction generator coupled to the first register and the second register that generates a set of error correction bits for the first number of bits and the second number of bits; a first data transmitter coupled to the first register and the error detection generator that transmits the first number of bits and the error detection bit; and a second data transmitter coupled to the second register and the error correction generator that transmits the second number of bits and the set of error correction bits. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but

Art Unit: 2112

is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 16, Liu et al. discloses the procedure for the claimed data transmission device of claim 15 wherein the error correction generator generates the set of error correction bits for the first number of bits, the second number of bits, and the error detection bit. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 17, Liu et al. discloses the procedure for the claimed data transmission device of claim 15 further comprising: a plurality of second registers that receives one of alike

Art Unit: 2112

plurality of the second number of bits; a like plurality of error correction generators, coupled to the first register and one of said plurality of second registers, each of said plurality of error correction generators generating a set of error correction bits for the first number of bits and one of said plurality of the second number of bits; and a like plurality of second data transmitters coupled to one of said plurality of second registers and one of said plurality of error correction generators to transmits one of said plurality of second number of bits and said set of error correction bits. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 18, Liu et al. discloses the procedure for the claimed data transmission device of claim 15 wherein the error correction generator is further coupled to the error detection generator and the set of error correction bits includes the error detection bit. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 19, Liu et al. discloses the procedure for the claimed data reception device comprising; a first register that receives a first number of bits and an error detection bit for the first number of bits; a first data available indicator; an error detector coupled to the first register and the first data available indicator, said error detector to detect a first error in the first number

Art Unit: 2112

of bits and to set the first data available indicator if the first error is not detected; a second register that receives a second number of bits different from the first number of bits and a plurality of error correction bits for the first number of bits and the second number of bits; a second data available indicator; and an error corrector coupled to the first register, the second register, the first data available indicator, and the second data available indicator, said error corrector to correct a second error in the first number of bits and the second number of bits, and to set the first and second data available indicators. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 20, Liu et al. discloses the procedure for the claimed data reception device of claim 19 wherein said error corrector further corrects the second error in the first number of bits, the second number of bits, and the error detection bit. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 21, Liu et al. discloses the procedure for the claimed data reception device of claim 19 wherein the error corrector further corrects one of the first error in the first number of bits, the second error in the second number of bits, and the second error in the error detection bit. {See Liu et al., Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig.

1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 22, Liu et al. discloses the procedure for the claimed computer data signal embedded in one of a machine readable device and a machine readable medium comprising: a first code group having a first symbol and a first code for the first symbol, the first code providing a first level of error protection for the first symbol; and a second code group that is transmitted after the first code group if the first code indicates an error in the first code group, the second code group having a second symbol different from the first symbol and a second code, the second code providing a second level of error protection for a third symbol that includes the first symbol and the second symbol; the second level of error protection being greater than the

Art Unit: 2112

first level of error protection. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 23, Liu et al. discloses the procedure for the claimed computer data signal of claim 22 wherein the first code is a single bit error detection code and the second code is an error correction code. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction

Art Unit: 2112

such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

As per Claim 24, Liu et al. discloses the procedure for the claimed computer data signal of claim 22 wherein the third symbol further includes the error detection code. {See **Liu et al.**, Fig. 1 and page 50 col. 2 para. 2 et seq., wherein data arrangement means (Fig. 1) is depicted for combining information data and a first code C0 and a second code C1 to provide error protection (Hybrid ARQ on page 51 col. 1 last two paras. Et seq.) with C0 and C1 being different, and C1 providing both error detection or correction.

For example, information data is sent with CRC detection means: when no error is detected via CRC detection means, the information is used as is. Otherwise, the receiver detects an error in the received information and requests additional info in the form of error correction such as an invertible RS or parity code from the sender along with CRC detection means appended thereto.

Upon receiving said invertible RS code, when no error is detected in said invertible RS or parity code via said appended CRC detection means, the receiver proceeds to allow correction of said formerly received information via utilization of said invertible RS or parity code to correct either the received information or the CRC detection means formerly attached thereto.

Otherwise, if an error is detected and is correctable, the receiver proceeds to allow correction on the RS or parity code..., and the information is accepted. If an error is detected but is uncorrectable, an ARQ is performed or in a storage medium, an equivalent reread or retry operation is initiated.}

CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E.
Primary Examiner
